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DATA-BASED LOAD PULL SIMULATION FOR LARGE-SIGNAL TRANSISTOR MODEL VALIDATION

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A new method for large-signal transistor model validation is described. Previous methods of large-signal model validation were performed without incorporating the effect of harmonic termination. The proposed method couples a harmonic-balance engine with measured automated load pull system S-parameter data at fundamental and harmonic frequencies. The load states are synchronized properly so that the transistor model is loaded in the simulation exactly as it is during load pull characterization. Measured vs. simulated results for a 1 mm GaAs MESFET at 2 GHz are presented.

A fundamental element of large-signal transistor model extraction is the establishment of its validity domain. This determination is best completed with a load pull system so that the measured contours of power, efficiency, and third-order intermodulation (IM3)/adjacent-channel protection ratio (ACPR) can be compared to those predicted by the model. Previously, a method was developed to simulate load pull contours using harmonic balance.[1] Although the method used measured load-tuner data at the fundamental frequency, it did not present the proper load impedance at the harmonic frequencies. This problem is not significant when the device's operating frequency is within a decade of f_t.[2] However, for situations when f_t is greater than a decade of the operating frequency, the error can be significant. From this condition, it is difficult to distinguish the source of error: the transistor model, the parameter extraction or the harmonic termination mismatch.

A new method for large-signal transistor model validation has been proposed. This method uses measured load-tuner S-parameter data at fundamental and harmonic frequencies, synchronized properly, to present load impedances exactly as seen by the device under test during load pull. Measured versus simulated results for a 1 mm GaAs MESFET device operating at 2 GHz are presented.

Proposed Method Theory

Validated large-signal transistor models are mandatory for nonlinear simulation. Validation is necessary to verify that the model is exhibiting an acceptable level of accuracy and to establish the load impedance domain over which this level of accuracy is maintained. For example, most large-signal models rely generally on nonlinear optimization to fit the model parameters to measured data. Since model parameters are a function of the system impedance in which the measured data were taken, usually 50 ohm, high SWR loading can impact model accuracy. Typically, high SWR loading would be encountered in RF power amplifier applications. Load pull is a rigorous method for characterizing this effect, particularly for high power, low voltage applications.

Classical load pull presents a range of arbitrary impedances to the device under test. A harmonic impedance is associated with each load state, which was ignored in previous load pull simulation methods.[1] The proposed method takes measured S-parameter files of fundamental and harmonic load impedances and sychronizes them properly for nonlinear simulation. Here, synchronization implies that the harmonic load states will correspond to the associated fundamental load state.

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Figure 1 shows a block diagram of the proposed method. The approach consists of two parts: a harmonic balance engine and a load-tuner block. The Microwave Design System™ was used to implement the described approach.[3] The load-tuner block accepts measured .slp files that represent fundamental and second- and third-harmonic load data. The load impedance is represented as

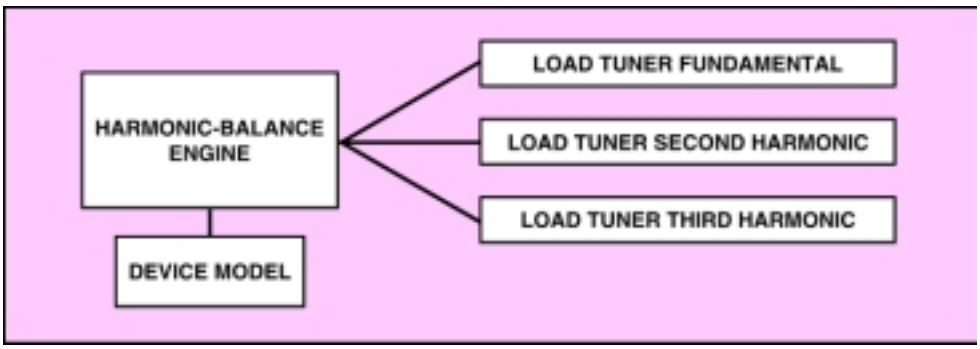

Figure 1: The proposed data-based load pull simulation method.

$$\Gamma_{load} = \begin{cases} \Gamma(f_0) & f < 1.5f_0 \\ \Gamma(2f_0) & 1.5f_0 < f \le 2.5f_0 \\ \Gamma(3f_0) & 2.5f_0 < f \end{cases} \quad (1)$$

where
f_0 = the fundamental frequency

These breakpoints are chosen to segregate the load states from one another, which is critical for load pull of IM3/ACPR. The proposed method is quite fast since harmonic balance uses previous solutions as a guess for a new simulation and each load state represents only a minor change from those adjacent to it.

Measured And Simulated Results

An EEFET-3 model was extracted for a 1 mm GaAs MESFET using static IV measurements and an HP 8510 network analyzer.[4] The extraction was performed in situ, with package parasitics extracted using a method described previously.[5] The device was load pulled at 10 V and $0.5I_{dss}$ at 2 GHz, with reference planes at the device leads. Approximately 30 load states were used with an automatic test systems.[6] A return loss of > -10 dB was maintained over the load pull domain. *Figure 2* shows measured versus simulated load states at the fundamental, second and third harmonic. Note that the agreement is good.

Figure 2: Measured and simulated load impedances for the (a) fundamental, (b) second-harmonic and (c) third-harmonic frequencies at 2 GHz.

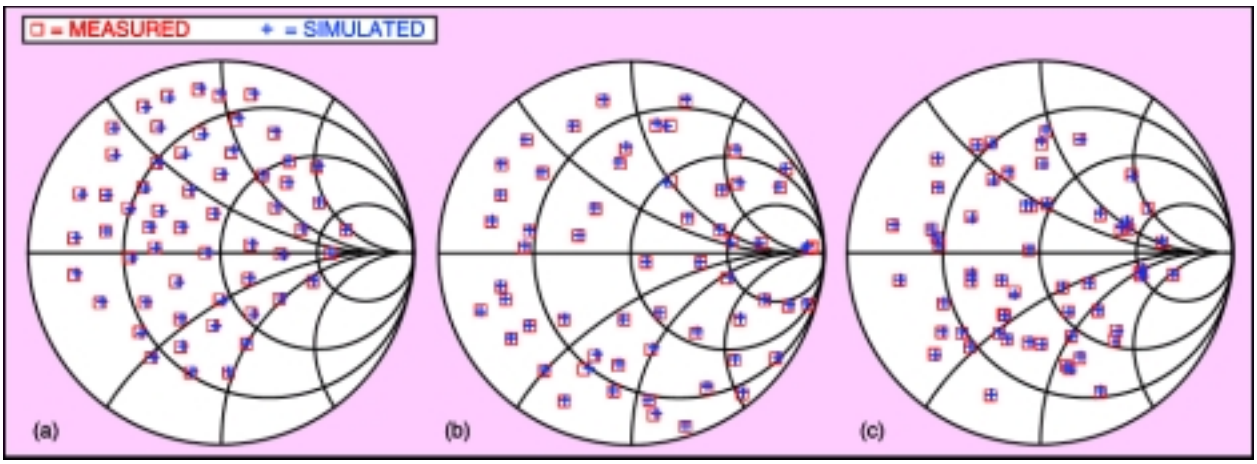

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Figure 3 shows measured and simulated load power and transducer gain. ***Figure 4*** shows measured and simulated drain efficiency. The loading was for maximum output power. The results are in good agreement, both in power back-off and compression. Measured load pull results for maximum load power produced a load impedance of 35 + j25 ohm. Using the proposed method, the simulated load pull produced a load impedance of 35 + j24 ohm, demonstrating good agreement. *Table 1* lists the measured and simulated results.

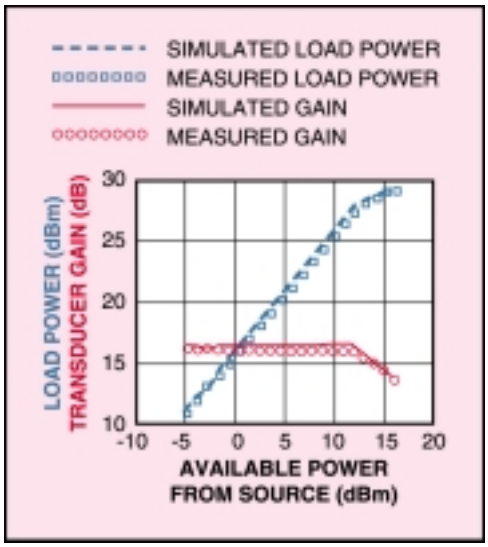

Figure 3 Measured and simulated load power and transducer gain.

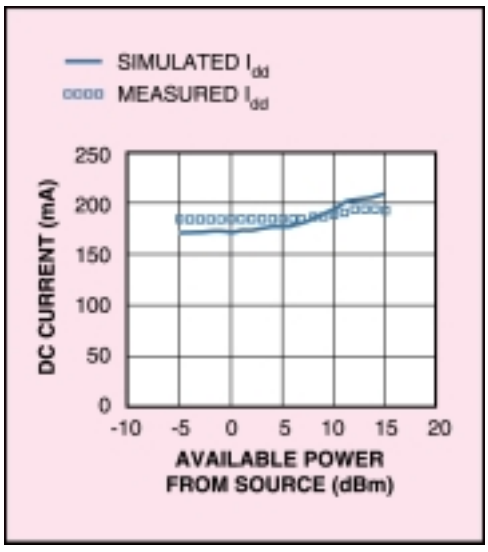

Figure 4 Measured and simulated DC input current.

TABLE I

MEASURED AND SIMULATED LOAD-PULL RESULTS

Parameter	Measured	Simulated
Maximum power (dBm)	29.0	28.9
Maximum gain (dBm)	15.0	14.9
Current at maximum power (mA)	239	217
Load impedance for maximum power (Ω)	35 + j25	31 + j24

Conclusion

A new method for validating large-signal transistor models has been proposed. The method is based on linking a harmonic-balance simulation engine representing measured fundamental and harmonic load impedances. Good agreement was obtained between measured and simulated results, demonstrating that the model was functioning properly. Future work will extend the present method to simulation of ACPR for the code-division multiple access (IS-95) standard using the circuit envelope simulation method.[3,7-9]

Acknowledgement

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