Improvements in High Power LDMOS Amplifier Efficiency Realized Through the Application of Mixed-Signal Active Loadpull

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Abstract — **This paper presents the results of experimental large-signal characterization of a high power LDMOS amplifier using a mixed-signal active load pull system. The architecture of the system provides the freedom to present unique and independent reflection coefficients at multiple different frequencies. In this case the fundamental frequency, and the 2nd harmonic frequency were chosen, and the reflection coefficients presented to the output terminal of the transistor were captured at these two frequencies. A high voltage LDMOS power amplifier from Freescale Semiconductor was studied and the results will demonstrate that a distinct improvement in drain efficiency is realized through careful magnitude and phase selection of the reflection coefficient at the 2nd harmonic frequency while keeping the refection coefficient presented at the fundamental frequency at a constant optimized value.**

Index Terms — **Loadpull, High Power Measurement, Harmonic Tuning, power amplifiers.**

I. INTRODUCTION

Loadpull systems that are used to characterize high-power transistors for wireless infrastructure applications continue to be based primarily on mechanical (passive) tuners [1]. This technique has been adopted as the standard for high power applications due to its simple nature compared to alternative approaches and the tuner's ability to handle high pulsed peak-power levels.

While passive tuners have many advantages one disadvantage is the lack of control over refection coefficients presented by the tuner at uncalibrated frequencies [2]. Passive tuners are designed to have very high quality factors which allow them to present a high refection coefficient to the device under test. This very desirable trait, however, reduces the tuning range to a very small frequency bandwidth [2]. Energy that is generated or reflected by the device under test (DUT) at the uncalibrated frequencies will be partially absorbed and partially re-reflected by the tuners in a manner that cannot be pre-determined. As a result, any changes to the devices behavior due to this stray energy could potentially lead to inaccurate device characterization or misunderstanding of device behavior [2].

Several innovative passive techniques that allow for calibration and impedance control at multiple frequencies (mostly the harmonic frequencies) have become commercially available over the past several years. These systems accomplish harmonic manipulation by adding additional tuners for each harmonic frequency either in cascade or through a network of filters in the form of a diplexer or triplexer [3,4].

In the case of cascaded tuners there are simply additional tuners (or resonators within the same tuner) that are placed between the DUT and the fundamental tuner. The cascaded resonators work in conjunction with each other to provide the desired refection coefficient magnitude and phase for each frequency of interest. The benefit of this approach is the relatively similar set up and operation compared to a standard passive loadpull configuration. The disadvantages are the increased insertion loss between the DUT and the fundamental tuner and poor isolation between the multiple resonators. High isolation between resonators within the same tuner can be achieved within very narrow bandwidths.

In the case of the diplexer/triplexer configuration multiple tuners are given a direct connection to the DUT via filters that direct the signals to the appropriate tuners based on frequency. The configuration of this system is relatively complicated and is limited to the availability of diplexers and triplexers that can be purchased for the frequency bands of interest. The benefit is highly isolated control of the harmonic frequencies with only small insertion losses.

While effective, these approaches require additional peripheral hardware and characterization time. Automated mechanical tuners with high gamma capabilities can also be expensive to purchase and maintain. Active load pull has become a popular choice for wide band and multi-harmonic tuning. Standard system architectures can support multiple frequency agnostic loops for tuning while stray energy generated within the system is terminated with the characteristic impedance of the system. Open loop active load pull systems are also capable of accommodating relatively large signal bandwidths due to the impedance being presented to the device under test being completely synthesized [2].

II. MIXED-SIGNAL HARMONIC LOADPULL

The high data traffic on today's cellular networks has created demand for a power amplifier that is both linear and efficient. LDMOS power amplifiers biased in class AB and class B offer acceptable theoretical efficiencies along with distortion products that can be sufficiently corrected using appropriate impedance matching or digital pre-distortion

techniques. Theoretical class AB and class B amplifier operation are only realized under the condition of the 2nd harmonic frequency be terminated in a short circuit. This condition will ensure that the output voltage and current waveforms are reduced to a sinusoid [5].

When analyzed in practical applications it has been found that achieving expected efficiency values from power amplifiers required some additional tuning that was not entirely explained in PA literature. The theory of Class J operation suggests that the high output drain-to-source capacitance (C_{ds}) could require an adjustment of the 2nd harmonic termination. In order to achieve the maximum efficiency for an amplifier operating with a significant output capacitance the ideal 2nd harmonic termination would need to be equal to the capacitive reactance of C_{ds} [5]. Therefore, to properly realize the entitlement of a LDMOS power amplifier operating in a high efficiency mode, the refection coefficients presented to terminate/load the device under test must be controlled at the fundamental and harmonic frequencies. Results have been demonstrated in previous experiments [6-7].

Active loadpull topologies have proven to be well suited for the task of harmonic tuning. Signals can be manipulated or synthesized to create a desired refection coefficient as easily at harmonic frequencies as they can at the fundamental frequency and active architectures terminate all out-of-band frequencies with the characteristic impedance of the system [8]. In the main drawbacks of active loadpull are the need for injection amplifiers that remain linear while producing the high output power needed to achieve large refection coefficients and operational complexity [8].

The technique of mixed-signal active loadpull has been effective in incorporating the architectural advantages of active loadpull into a single unified measurement system [9]. The term "mixed-signal" refers to a process in which a signal is generated at a low base-band frequency and then segmented in the time domain into several new signals that are then manipulated in terms of frequency, magnitude, and phase. These new signals are simultaneously injected into the device creating new "*a*" waves that change the refection coefficient. The system loads refection coefficients measured from the device into a wide band analog to digital converter (ADC). The desired injection signals are then computationally generated in the base band, up converted to the desired frequency using IQ up conversion, and injected into the device using arbitrary wave form generators (AWG's). Because the wide band ADC can sample thousands of refection coefficients from the DUT, and the AWG's supplying the injection signals are phase coherent, large multi-dimensional sweeps are possible within a single measurement iteration making the mixed-signal approach the superior architecture in terms of speed [10]. Furthermore, by utilizing the open loop architecture and methods of IQ signal up conversion, the mixed-signal approach can control refection coefficients over

a wide frequency bandwidth making it ideally suited for large modulation band width applications [11].

III. MEASUREMENT CONFIGURATION

Multi-harmonic on-wafer measurements were performed on a Freescale high voltage LDMOS power amplifier with a 2.4mm gate periphery at a fundamental frequency of 2GHz. A block diagram of our measurement test set is shown in Fig. 1. As shown in Fig. 2, the DUT was laid out in a ground-signal-ground (GSG) configuration. In this configuration the active device was physically connected to a gate and drain manifold which were then connected to a short transmission line and eventually a probe pad. Additional ground pads were placed on each side of the signal pad on both the gate and drain. The pads were configured in order to accommodate on-wafer probes with a 150um signal-to-ground pitch. It is critical to choose probes with high power handling capability, low insertion loss, and low contact resistance [12].

Our objective is to capture and understand the RF performance accurately by characterizing the active area of the transistor. To achieve this several stages of de-embedding needed to be applied as shown in Fig.3.

A TRM vector calibration was performed to remove all magnitude and phase characteristics of passive elements such as cables, connectors, and probes between the measurement system reference ports and the probe tips [8]. On-wafer GSG calibration standards, provided by the probe manufacturer, were measured to obtain the necessary error coefficients.

An absolute power calibration was performed to obtain the correct amplitude of measured data. A phase reference calibration was performed to ensure the correct relationship between the fundamental frequencies and the harmonic frequencies were obtained. Determining this relationship is a necessary step if time domain waveforms are to be constructed from the frequency domain measurements [8].

The second stage of de-embedding involves removing the effects of the GSG probe pads and the transmission line connecting the signal probe pad to the device manifold. This will shift the reference plane to the green line in Fig.3. The two port network characteristics of these passive components were determined by measuring the s-parameters of a GSG thru structure that exactly represents the length and width of the two transmission lines leading up to the device manifold. Once the admittance parameters of this structure are known it is possible to numerically 'split' the through in half and obtain a two-port network representation of each side [13]. It has been shown that this technique yields results similar to alternative techniques for on-wafer de-embedding [14].

The final stage of de-embedding is the removal of the device manifold characteristics. This step will shift the measurement reference plane to the active device as shown by the red line in Fig.3. The two-port network parameters of these structures are represented with an electromagnetic simulation as it would be very costly to have such large calibration

structures printed inside each reticule of a wafer. Sonnet *em* is a well suited tool for this task as it allow for fast simulation of symmetrical structures [15]. This tier of de-embedding will shift our measurement reference plane to the extrinsic network of the transistor.
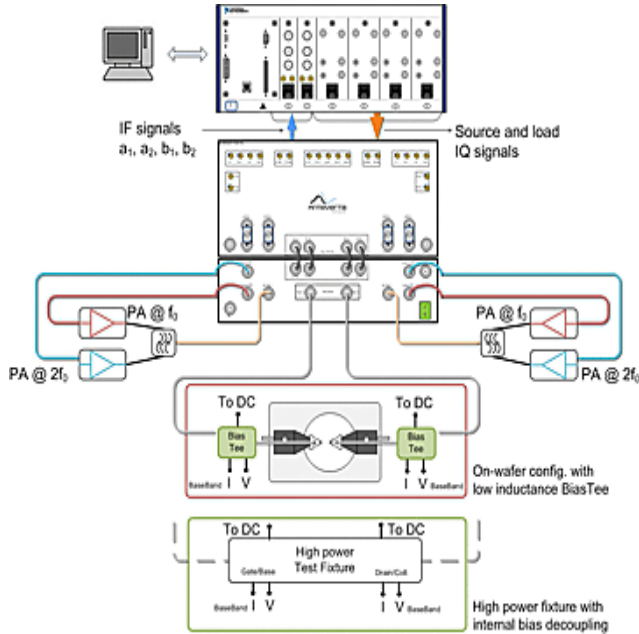

Fig. 1.   Block diagram of the mixed-signal active load pull system used for this characterization. Image courtesy of Maury Microwave.
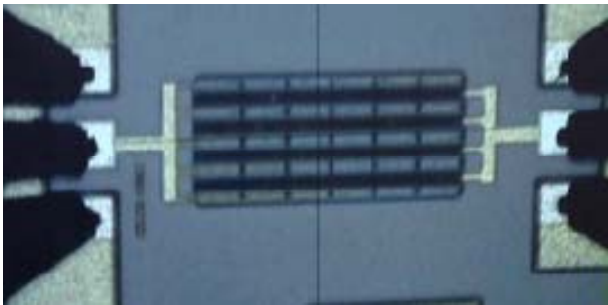

Fig. 2.   Image of a 5mm LDMOS power amplifier in ground-signal-ground (GSG) configuration. The device in this image is in a similar configuration to the 2.4mm device that was measured in this experiment. The measurement reference plane was at the tip of the probes. The effects of the probe launch, device manifold, and the device's extrinsic network were included in the measured data.
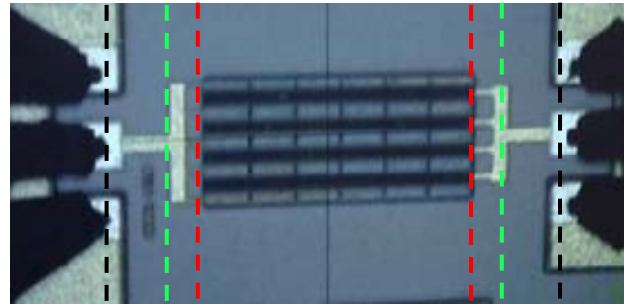

Fig. 3.   Image of a device similar to our DUT in the GSG configuration illustrating the measurement reference plane obtained after applying each stage of de-embedding. The black lines at the probe tips show the reference plane after performing the on-wafer TRM vector calibration. The green lines show the reference plane after applying the s-parameters of the GSG launch obtained by mathematical separation of the on-wafer thru structure. The red lines show the reference plane after applying the s-parameters of the manifolds obtained by electromagnetic simulation. The measurements were performed at the probe tip reference plane (black line) and measured data was post processed to obtain results at the active device reference plane.

IV. RESULTS

A highlight feature of the mixed-signal active load pull system is the speed at which the data is acquired. We started by selecting 39 load impedance points at the fundamental frequency and performing an input power sweep with 12dB of dynamic range. The system was able to complete this measurement plan, which consisted of 468 points, in less than one minute. A plot of output power vs. input power for all measured sweeps is shown in Fig.4. From this first set of data we were able to choose the optimum fundamental load impedance which is the basis for our harmonic measurements.

Class-J amplifier literature suggests that we will see an improvement in drain efficiency when the load impedance at the 2nd harmonic becomes inductive enough to match the output capacitance of the transistor. As shown in Fig.4 we rotated the phase of our 2nd harmonic load impedance while keeping it's magnitude very high and keeping the fundamental load impedance at the constant value.

Fig.5 shows output power vs. input power at significant 2nd harmonic phase angles.Fig.6 shows a plot of drain efficiency vs. the phase of the 2nd harmonic load. We experienced an increase in drain efficiency of approximately 10% when the phase of the 2nd harmonic load impedance was approximate equal to 80°. Fig.7&8 show the time domain waveforms at significant 2nd harmonic phase angles.
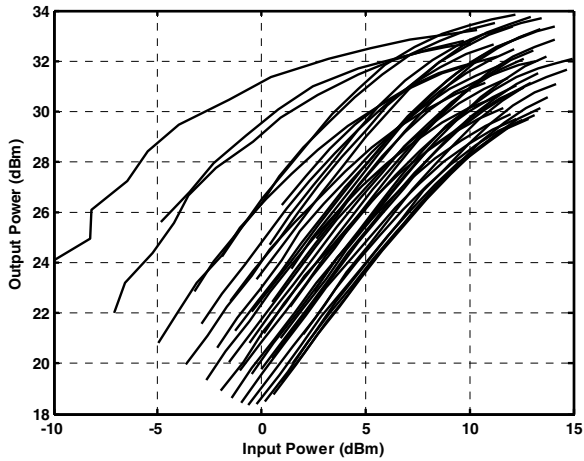
Fig.4. Plot of output power vs. input power for data captured during fundamental tuning of a 2.4mm on-wafer LDMOS device from Freescale Semiconductor using the mixed-signal active loadpull system. A total of 460 indiviual measurement points were captured in less than one minute
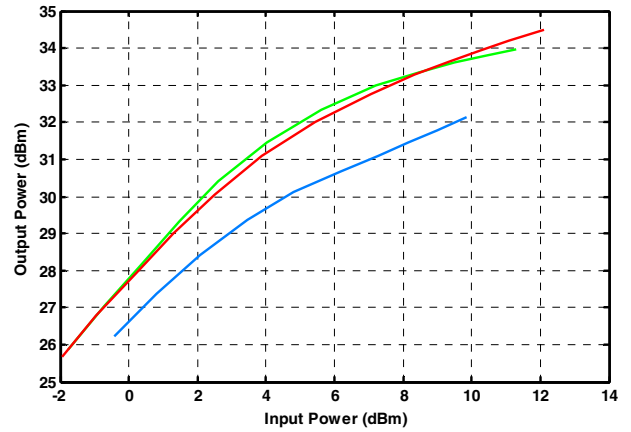
Fig. 5. Plot of measured output power versus input power at the 2nd harmonic load terminations highlighted in Fig. 3. The color of the traces in this plot map directly to the terminations plotted in Fig. 3.
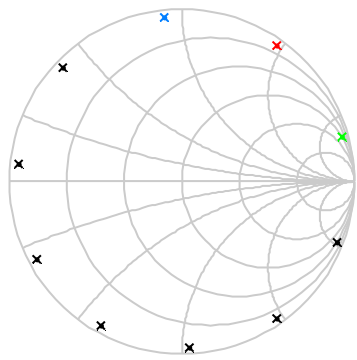

Fig. 5. A smith chart representation of the 2nd harmonic measurement plane. The three colored dots represent terminations of high interest which are referred to in subsequent figures. The termination in blue resulted in the highest values of drain efficiency and output power. The termination in red resulted in values of power and efficiency that were much lower than then expected in standard operation. The termination in green resulted in standard performance of the device. The black dots represent other measured points that resulted in performance comparable to that of the green trace and would be considered typical for this device.
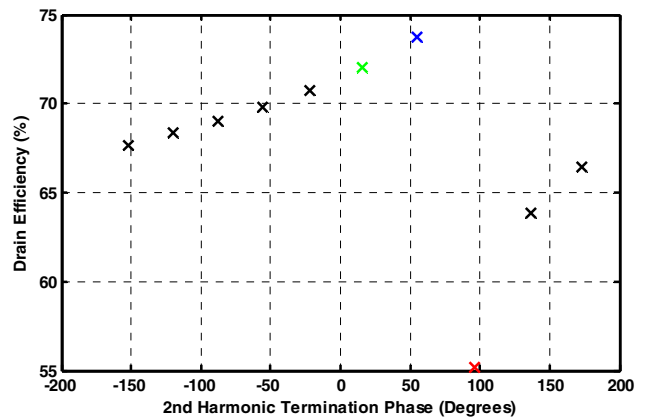
Fig. 6. A plot of measured drain efficiency verses 2nd harmonic load termination phase. The color of the traces in this plot map directly to the terminations plotted in Fig. 3. The efficiency measurements were taken at 3dB transducer gain compression point.
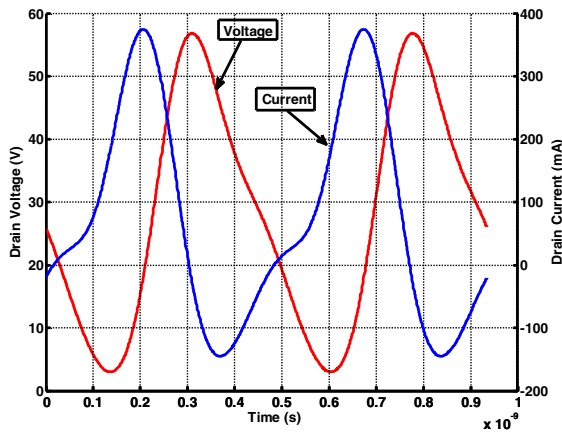
Fig. 7. Phase synchronous time domain plot showing drain voltage versus drain current at the load termination with the highest drain efficiency. This plot was collected as part of our evaluation without any additional time expense.
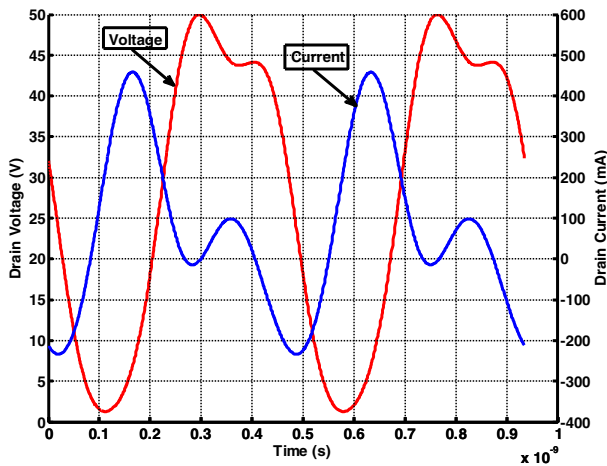

Fig. 8. Phase synchronous time domain plot showing drain voltage versus drain current at the load termination with the lowest drain efficiency. This plot was collected as part of our evaluation without any additional time expense.

V. CONCLUSION

We have discussed the importance of harmonic tuning as it applies to high efficiency LDMOS power amplifier operation. We have discussed various harmonic loadpull options including their strengths and drawbacks. We discussed in detail the features of mixed-signal active loadpull and the advantages of this technique which include enhanced measurement speed and the ability to evaluate devices in extremely wide band applications. Finally we have shown a very practical application of the mixed-signal technique for quickly evaluating the entitlement of an LDMOS amplifier under optimum harmonic loading conditions with the measurement reference plane set to the extrinsic network of the transistor. From an organizational standpoint this technique is extremely useful as it provides a rapid approach to advanced device characterization which will ultimately lead to a reduced design cycle-time.

VI. ACKNOWLEDGEMENTS

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