On the Second-Harmonic Null in Design Space of Power Amplifiers

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***Abstract*— This letter investigates the source of performance degradation and efficiency null that is traditionally observed during second-harmonic load pull of active power transistors. A theory that explains the performance degradation is presented, resulting in a simplified closed-form equation that predicts the location of performance null for different device peripheries and/or design frequencies. Thereafter, the intrinsic drain waveforms for null and maximum efficiency are analyzed to study potential causes for efficiency degradation. The theory is validated using active load-pull measurements of laterally diffused metal–oxide–semiconductor and gallium nitride active devices for different peripheries (0.5–4.8 mm) at various frequencies of operation (2, 2.6, and 3.5 GHz).**

***Index Terms*— Active load pull (ALP), efficiency null, harmonic tuning, power amplifiers (PAs), second harmonic.**

I. Introduction

THE base station power amplifier (PA) designs for massive multiple input and multiple output applications are focused on improving achievable efficiency by manipulating harmonics. Harmonically tuned amplifiers rely on precisely tuning or setting fundamental and harmonic impedance levels presented to the active device to improve performance [1], [2]. As part of the design process, PA designers often rely heavily on computer-aided design simulations or load-pull measurements to evaluate such tradeoffs and estimate the level of performance that can be achieved for a given technology, device size, operating voltage, and frequency. At any given harmonic impedance location, maximum efficiency and power can be observed for a given output power or compression level. In general, a second-harmonic load pull shows a region on the Smith chart wherein performance degrades quite significantly. This efficiency degradation has been quite extensively reported in the literature for different frequencies and devices [3]–[6]. This degradation (efficiency null) poses a significant challenge in the selection of a second-harmonic output match by reducing the available area for the second-harmonic match. This region graphically illustrated in Fig. 1(a) is often considered critical and usually avoided by designers to maximize PA performance [3]. Although this phenomenon is widely known, the actual reason behind the efficiency degradation has not been addressed in previous works.

This letter proposes an explanation for this abovementioned behavior that is confirmed by theoretical and measured results. A new closed-form equation is derived for predicting the location of the efficiency null for any device periphery and frequency of operation. Because the proposed equation relates the output parasitic capacitance of a device to where efficiency null occurs, it can be used as a simple yet accurate means for predicting the output capacitance of the device as well as its optimal impedance points at the current-generator plane. This valuable information (typically not available from device vendors) can be used to study the intrinsic operation of the PA in terms of voltage and current waveforms, which further increases the chances of achieving a first-pass design with maximum performance.

This letter is organized as follows. In Section II, the theoretical postulation of efficiency null is presented to explain the causes of degradation in efficiency. Thereafter, active load-pull (ALP)-based measurements are presented in Section III to validate the proposed theory. Conclusions are presented in Section IV.

II. Second-Harmonic Null: Theoretical Analysis

With fundamental impedance at maximum power load (MXP) of device ($R_{\text{opt, MXP}} = (V_{dc} - V_k)/I_m$), the second-harmonic load sweep (i.e., changing the phase at $2f_o$) shows performance degradation in terms of output power, drain efficiency, and gain as reported in Fig. 1(b). This efficiency degradation or null location changes from device to device and lacks a clear theoretical formulation in terms of its predictability and the possible cause of its occurrence.

A. Theoretical Postulation of Efficiency Null

The phase of efficiency null at second harmonic ($\sphericalangle\eta_{\text{null},2f}$) corresponds to the impedance at which the drain-to-source capacitance (C_{ds}) resonates with the second-harmonic impedance presented at the load of the device to create an open circuit at $2f_o$. Assuming a reactive second-harmonic impedance (jy_2) is presented to the device, the second-harmonic impedance can be written in terms of characteristic

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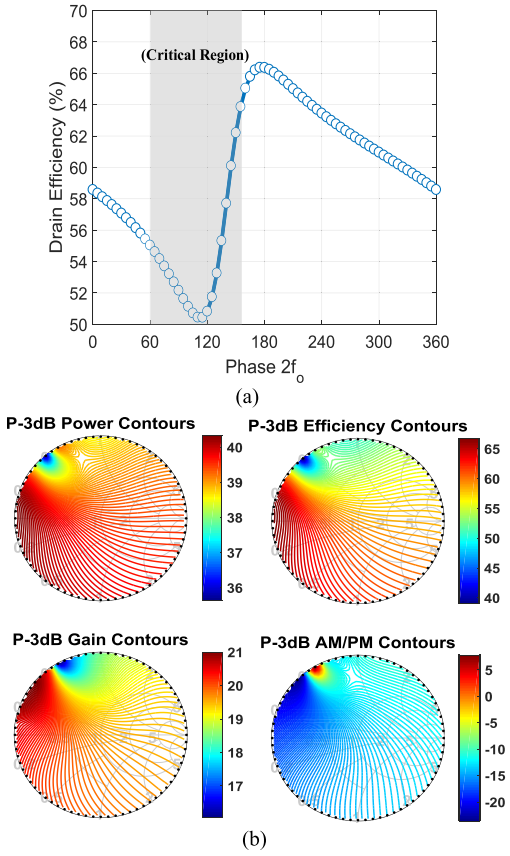

Fig. 1. (a) Second-harmonic load pull showing critical region for Class-B amplifier with fundamental load ($R_{\text{opt,MXP}}$) for maximum output power. (b) Output power, drain efficiency, gain, and AM/PM contours at 3-dB compression versus second-harmonic load pull for Class-B amplifier with fundamental load $R_{\text{opt,MXP}}$.

impedance (Z_o) as

$$\Gamma_{2f_o} = -\left(\frac{Z_o^2 - y_2^2}{Z_o^2 + y_2^2}\right) + \frac{2jy_2Z_o}{Z_o^2 + y_2^2}. \tag{1}$$

Using (1), the phase for the second-harmonic load can be expressed as a tangent function of y_2 and Z_o as

$$\sphericalangle\Gamma_{2f_o} = \tan^{-1}\left(\frac{-2y_2Z_o}{Z_o^2 - y_2^2}\right). \tag{2}$$

Since for fundamental impedance at $R_{\text{opt, MXP}}$, C_{ds} resonates out with y_2 at $2f_o$ creating an open-circuit condition, the phase of second-harmonic null ($\sphericalangle\eta_{\text{null},2f_o}$) can be theoretically formulated by substituting y_2 as a function of f_o and C_{ds} in (2) and can be evaluated as

$$\sphericalangle\eta_{\text{null},2f_o} = \tan^{-1}\left(\frac{\frac{-2Z_o}{4\pi f_o C_{ds}}}{Z_o^2 - \frac{1}{(4\pi f_o\ C_{ds})^2}}\right). \tag{3}$$

As one can infer from (3), the location where efficiency null occurs at a specific phase of second harmonic is dependent on C_{ds} and the operational frequency (f_o) for different technologies, such as laterally diffused metal–oxide–semiconductor (LDMOS) and gallium nitride (GaN). Efficiency null occurs near low-impedance region (or short reactive impedance) for large periphery devices and, on the contrary, near high-impedance region (or open-circuit impedance) for small

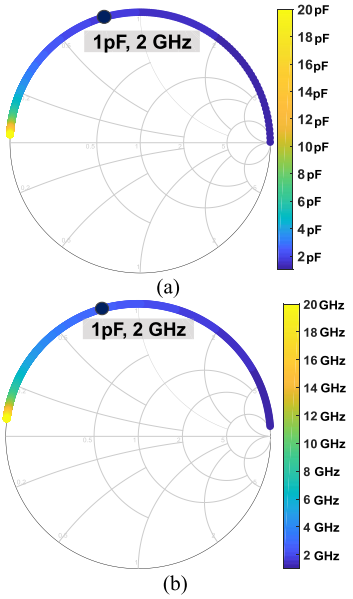

Fig. 2. Movement of null point with change in (a) periphery for fixed frequency of 2 GHz and (b) operational frequency for drain–source capacitance of 1 pF using (3) with $Z_o = 50\ \Omega$.

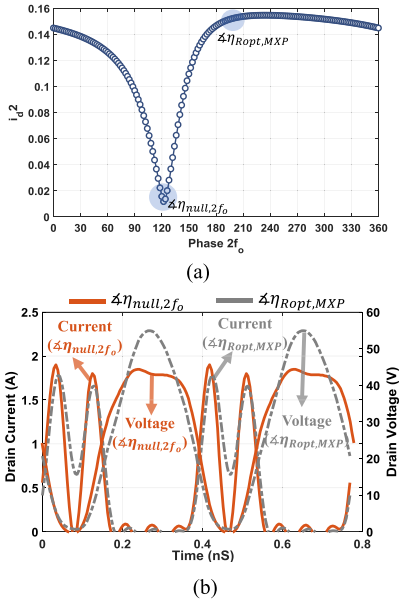

Fig. 3. For an LDMOS 4.8-mm device at 2 GHz with $Z_o = 50\ \Omega$. (a) Second-harmonic drain current as a function of phase of second-harmonic impedance. (b) Intrinsic drain waveform at phase $2f_o = 120°$ (red lined) and phase $2f_o = 180°$ (gray line).

peripheries. Likewise, at higher frequencies, the null occurs near short-circuit impedance and for low frequencies, it is near high impedance as depicted graphically in Fig. 2(a) and (b), respectively. While considering up to three harmonics at 2 GHz for a 4.8-mm LDMOS device, fundamental loading at $R_{\text{opt,MXP}}$ (best power load), the second-harmonic drain current is heavily impacted at $\sphericalangle\eta_{\text{null},2f_o}$ (minimum efficiency load). The open harmonic condition forces intrinsic second-harmonic drain current (i_d2) to be significantly small (almost zero) as shown in Fig. 3(a). Since the second-harmonic impedance is open circuit, even a small i_d2 creates a large-second-harmonic voltage component which widens the voltage waveform.

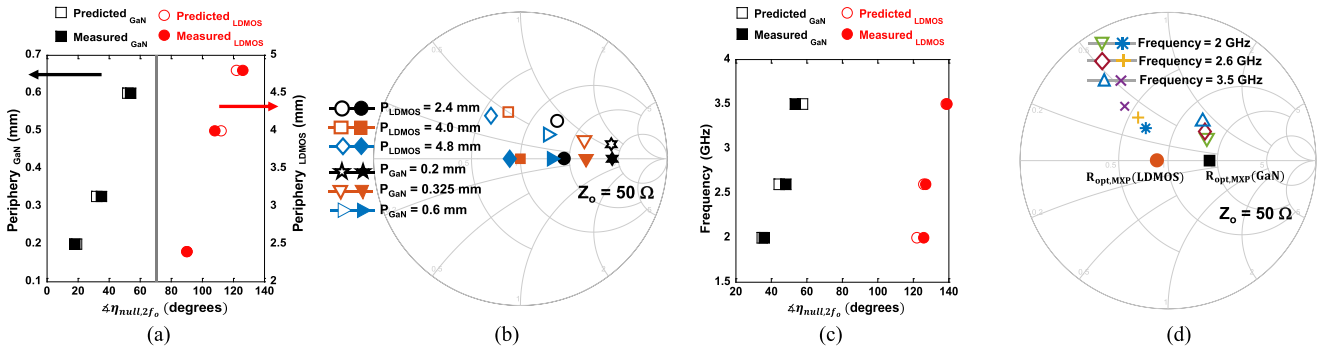

Fig. 4. Phase of second-harmonic null ($\sphericalangle\eta_{\text{null},2f_o}$) versus (a) periphery at 2 GHz. (b) De-embedded $R_{\text{opt,MXP}}$ using the GSG launch effects and C_{ds} extracted using $\sphericalangle\eta_{\text{null},2f_o}$. Shallow and filled markers represent probe and intrinsic planes, respectively. (c) Phase of second-harmonic null versus frequency for LDMOS (4.8 mm) and GaN (0.5 mm). (d) De-embedded $R_{\text{opt,MXP}}$ versus frequency for 4.8 mm (LDMOS) and 0.5 mm (GaN), respectively.

Furthermore, significant drop in $i_d 2$ also impacts the dc and fundamental drain current, thereby impacting the drain current waveform. The impact on drain current and voltage waveforms increases the overlap, thus decreasing the dc-RF conversion efficiency in the null region for an active device as shown in Fig. 3(b). On the contrary, for MXP fundamental loading, the maximum efficiency is achieved near short-circuit condition and is a safe region for PA design.

III. Experimental Validation Using Active Load Pull

To validate the theoretical postulation described in Section II, measurements are performed for different peripheries of LDMOS and GaN power devices at multiple frequencies using Maury's ALP system setup [7]. The data were measured at the probe tip and a two-tier de-embedding was used. The gate–source–gate (GSG) launch effects were de-embedded using a measured THRU calibration structure. Thereafter, using the periphery information, C_{ds} was de-embedded to measure the location of these impedances at the current-generator plane.

A. Movement of Null With Device Periphery (P)

At a frequency of 2 GHz, different periphery devices were probed at a drain–source voltage of 28 V at Class-B bias and second-harmonic load pull was performed with fundamental impedance fixed at $R_{\text{opt, MXP}}$ for both LDMOS (2.4, 4, and 4.8 mm) and GaN (0.2, 0.325, and 0.6 mm) devices. Subsequently, $\sphericalangle\eta_{\text{null},2f_o}$ was measured and compared with the theoretical prediction given by (3) and is reported in Fig 4(a). As can be inferred from Fig. 4(a), the theoretical null prediction is very close to the one measured using the ALP and the location moves toward short (180° with an increase in the periphery as predicted in Fig. 2(a). Once the location of null is known, the information can conversely be used to extract the large signal C_{ds} using (3). Thereafter, the $R_{\text{opt, MXP}}$ at probe pad and intrinsic plane are de-embedded for different peripheries using large signal C_{ds} and is reported for different peripheries in Fig 4(b). The impedances are also validated using intrinsic nodes available from NXP models and it perfectly aligns with C_{ds} estimation proposed in this letter.

B. Movement of Null With Frequency

For a 4.8-mm LDMOS and 0.5-mm GaN device, the theoretical angle predicted by (3) and measured null angle for different frequencies (2, 2.6, and 3.5 GHz) show a close agreement as reported in Fig. 4(c). With the increase in frequency, the location of null moves toward low impedance region as predicted by Fig. 2(b) of Section II. Using the null location, the estimated C_{ds} is used to de-embed $R_{\text{opt, MXP}}$ at intrinsic and pad planes for different frequencies and is shown in Fig. 4(d). The measurements agree quite well with the theoretically predicted values.

IV. Conclusion

This letter presents an explanation for performance degradation that is observed during second-harmonic load pull of active power devices. A closed-form equation is developed that provides an estimate of the exact location of the null based on the periphery and frequency of operation. Using the null location, PA designers can estimate the large signal C_{ds} of the device or vice versa. Measurements carried out using ALP system on LDMOS (2.4, 4, and 4.8 mm) and GaN devices (0.2, 0.325, and 0.6 mm) at different frequencies are in excellent agreement with theory. The prediction model provides accurate information about location efficiency null which agrees well with second-harmonic load pull.

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