On-wafer GaN Power Semiconductor Characterization

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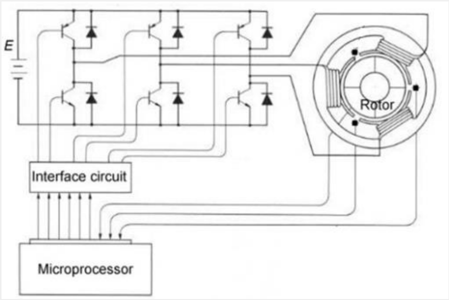
Agenda

1. Introduction
2. Setup
3. Measurements for System Evaluation
4. Measurements on DUT
5. Conclusion

Introduction – HV Switch Applications



For use in switching circuit applications

- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives

Key Parameters:

- I_{DSS} (Output current saturation)
- $V_{DS\ Max}$ (Avalanche ruggedness)
- $R_{DS\ (ON)}$ (System efficiency and reducing cooling requirement)
- Q_g (Low capacitance for max switching speed)

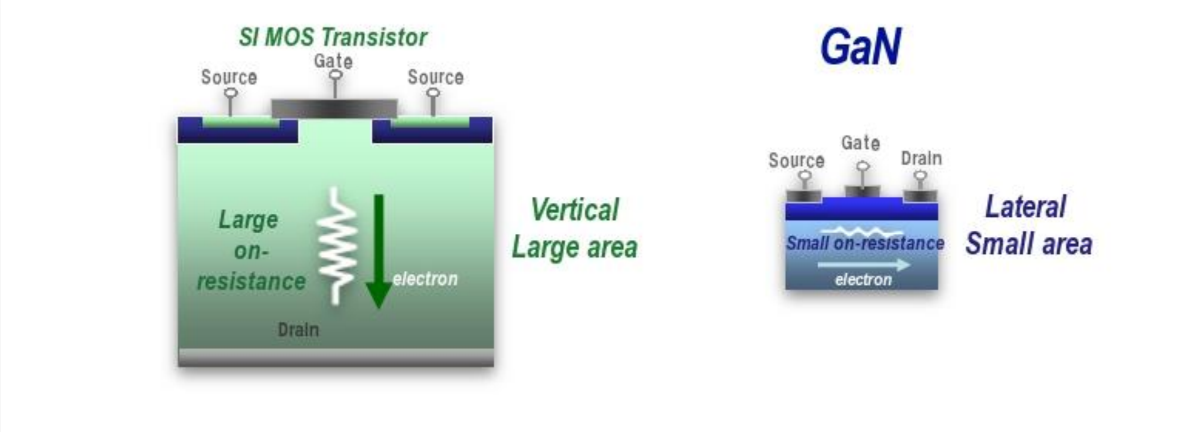
  - ➢ Measurement of these parameters in pulsed mode (close to switching operating conditions)
  - ➢ Influence of quiescent bias (evaluation of parasitic effects)

Introduction – GaN for HV Switches

"GaN has the potential to reduce energy loss of the power devices. GaN (gallium nitride), a compound of Ga (Gallium) and N (Nitrogen), possesses high breakdown voltage and low conduction resistance characteristics that enable high-speed switching and miniaturization.

Unlike conventional Si transistors that require bigger chip area to reduce on-resistance, GaN devices having small sizes (i.e. low parasitic capacitance) allow high speed switching and miniaturization with ease."

- Panasonic, 9/4/2014, http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/



Introduction – GaN for HV Switches

"GaN possesses many properties that make it an ideal material for power conversion devices. Its performance is substantially superior to silicon, and it is more cost effective than other compound power semiconductors such as silicon carbide.

-Wider Band Gap Reduces On-Resistance at High Voltage
-Higher Electron Mobility Enables Faster Switching
-High Temperature Capability for Improved Reliability
-Lower Cost — Can Be Grown on Silicon Substrates

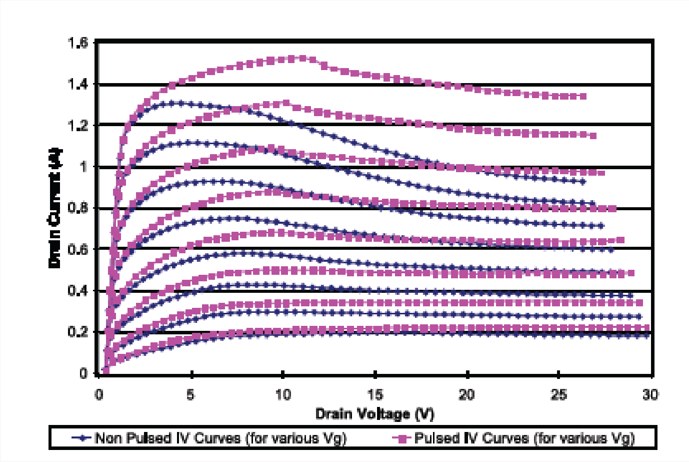
GaN-based power devices can achieve a specific on-resistance that is 100 times lower than silicon super junction transistors and even 10 times lower than SiC transistors. This enables much smaller die size, lower output capacitance, higher efficiency, and faster switching — ultimately leading to major system cost savings and smaller board footprints."

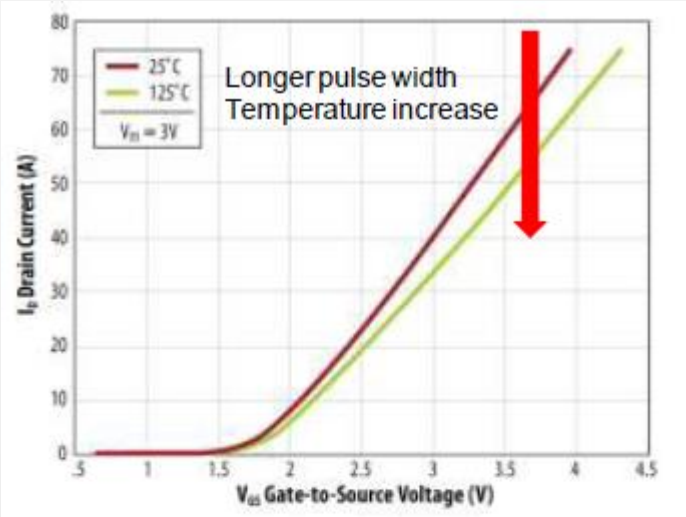
- *RFMD, 9/4/2014, http://www.rfmd.com/products/powerconversion/*

Introduction – Challenges with GaN

Self-Heating

- Device self-heating distorts data and prevents accurate device characterization when pulses are too long.
- Devices designed to target low conduction loss, which result in lower voltages across the device.
- Test equipment must be capable of generating high current and measuring low voltages in short time period.
- Pulsed measurements with short pulse width (~µs) is required to avoid device self heating especially for medium current at high voltage bias.
- The aim is to limit the maximum power using pulse stimulus

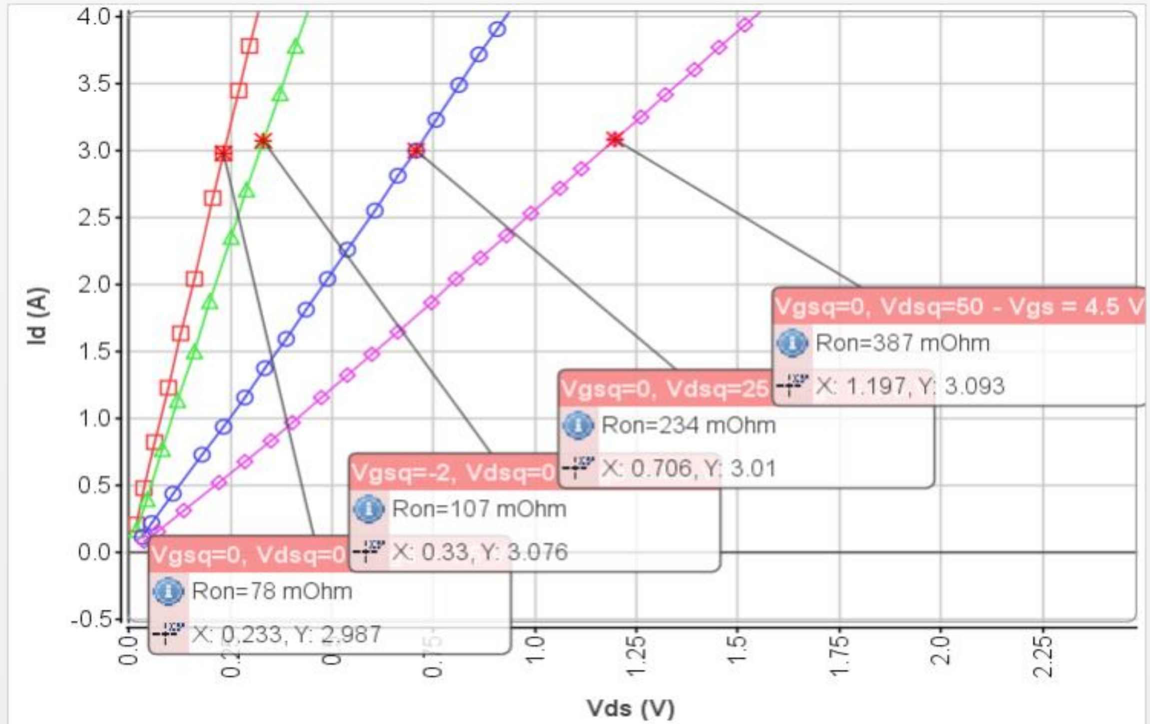




Introduction – Challenges with GaN

Parasitic Effects - Trapping

- Some technologies such as GaN transistors have some parasitic effects such as trapping effects.
- They can be highlighted by pulsed measurements. The quiescent bias point can influence the R_{on} characteristic for example.
- Pulsed measurements can be used to evaluate R_{on} as a function of the quiescent bias (I_{DS}=3A)



Ron (Vgsq=0, Vdsq=0) = 78 mOhms
Ron (Vgsq=-2V, Vdsq=0) = 107 mOhms
Ron (Vgsq=0, Vdsq=25) = 234 mOhms
Ron (Vgsq=0, Vdsq=50) = 387 mOhms

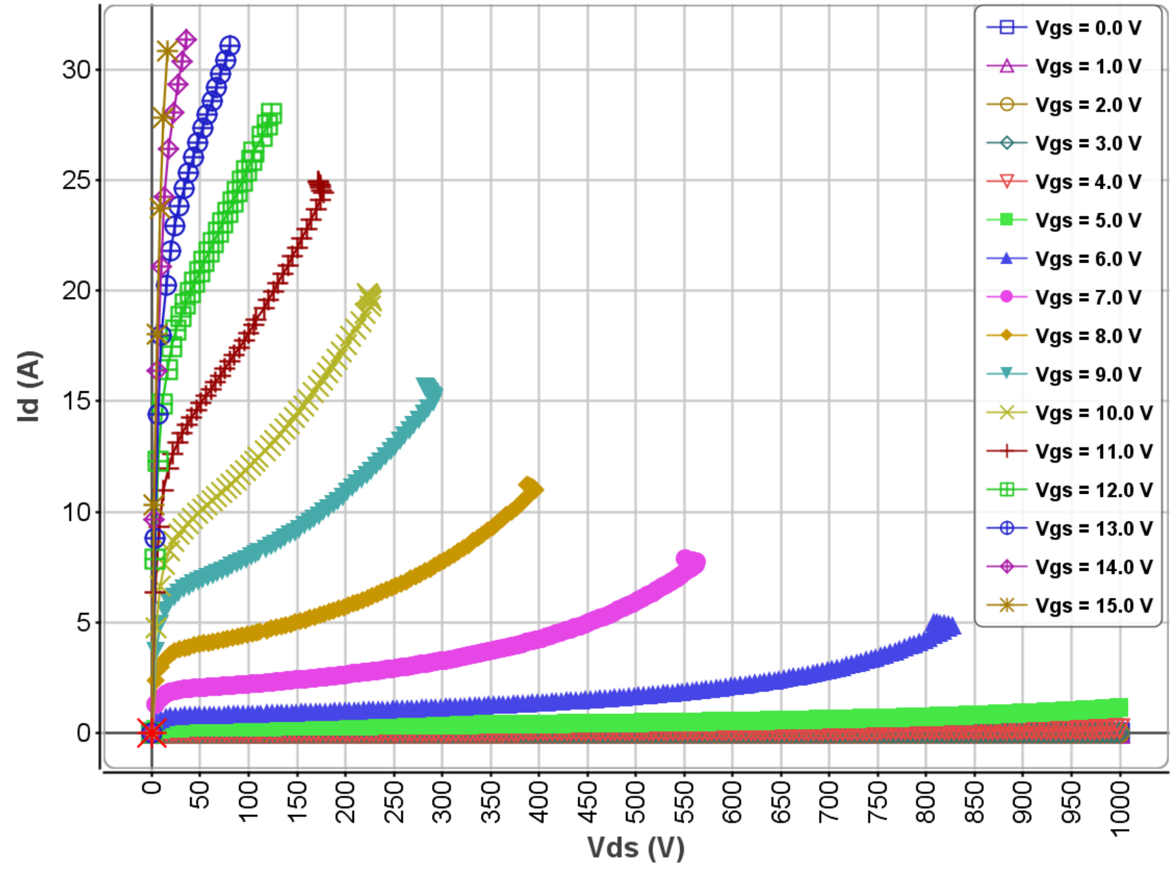
Introduction – Challenges with GaN

Breakdown Voltage

- Because of the high voltage capabilities, this system can be used to determine the breakdown voltage of device under tests.
- Quiescent point can be varied

The aim is to highlight the influence of the quiescent bias point under pulsed measurements on key parameters:

- I_{DSS}
- $V_{DS\ Max}$
- $R_{DS\ (ON)}$



Introduction – How to Characterize?

- Existing Pulsed IV / Parametric Analysis equipment with sufficient voltage/current capabilities have insufficient pulsewidth capabilities, on the order of 10µs or higher whereas 1µs or less is preferable for GaN

- Existing Pulsed IV / Parametric Analysis equipment can achieve high voltage OR high current, but not both simultaneously. How to test conditions of high P=VI?

- Existing on-wafer probes exist for high voltage OR high current, but not both. How to reduce inductance in probes to eliminate overshoots/ringing?

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