Transistor Compact modeling using IVCAD
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Model Schematic

- Based on 18-element
- Compatible with ADS and MO
Transistor Compact modeling using IVCAD

**Measurement System**

- **Short pulse**: Quasi-isothermal conditions
- **Low duty cycle**: Constant mean temperature
- **Quiescent bias point**: Thermal conditions fixed

**Advantages**

- High power dissipated areas // safe operating conditions
- Thermal effects: influence of QP on Idss
- Trapping effects (gate lag, drain lag)
- Precious modelling data inputs
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Compact modeling flow

Small-Signal

Non-linear capacitances

IV Model

Thermal model

Trapping effects

Rs, Rd

\[ y = 0.0029x + 0.6375 \]
\[ y = 0.0049x + 0.6889 \]

\[ 0.4 \quad 0.6 \quad 0.8 \quad 1 \quad 1.2 \quad 1.4 \quad 1.6 \]

\[ 0 \quad 50 \quad 100 \quad 150 \quad 200 \]

\[ T \, ^\circ\text{C} \]

Ri

─

Cds

τ

Gm

Gd

Cgs

Cgd

Dgs=f(Vgs)

Dgd=f(Vgd)

\[ \text{Cgs}=f(Vgs) \]

\[ \text{Cgd}=f(Vgd) \]

\[ \text{Dgs}=f(Vgs,T) \]

\[ \text{Dgd}=f(Vgd,T) \]

\[ \text{Ids}=f(Vgs,Vds,T) \]

\[ \text{Rs}=f(T) \]

\[ \text{Rd}=f(T) \]

\[ \text{Ids}=f(Vgs\_\text{trap},Vds,T) \]

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Compact modeling flow: Extraction of the linear model

- Small-Signal
  - Ri, Cds
  - Cgs, Cgd, Rgd

- Non-linear capacitances
  - Dgs=f(Vgs)
  - Dgd=f(Vgd)
  - Cgs=f(Vgs)
  - Cgd=f(Vgd)

- IV Model
  - Ids=f(Vgs, Vds)

- Thermal model
  - Dgs=f(Vgs, T)
  - Dgd=f(Vgd, T)
  - Ids=f(Vgs, Vds, T)

- Trapping effects
  - Rs=f(T)
  - Rd=f(T)
  - Ids=f(Vgs_trap, Vds, T)

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Compact modeling flow: Extraction of the linear model

Linear Model optimization

Multi-biasing extraction methodology of the linear model

There is only one set of extrinsic parameters for which intrinsic parameters are independent from the frequency.

For a given set of extrinsic parameters, intrinsic admittance matrix of the device is extracted from measured [S] parameters.
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Compact modeling flow: Extraction of the linear model

STEP 1: COLD FET MEASUREMENTS (Optional):

Vgs: Channel Open; Vds=0V

Shottky junction conduction @ Vds=0V

\[ Rs = \text{real}(Z_{21}) - \frac{R_c}{2} \]
\[ Rd = \text{real}(Z_{22}) - \text{real}(Z_{21}) - \frac{R_c}{2} \]
\[ R_g \approx \text{real}(Z_{11}) - \text{real}(Z_{21}) + \frac{R_c}{6} \]

\[ L_s = \text{Im}(Z_{21}) / W \]
\[ L_d = (\text{Im}(Z_{22}) - \text{Im}(Z_{21})) / W \]
\[ L_g = (\text{Im}(Z_{11}) - \text{Im}(Z_{21})) / W \]
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Compact modeling flow: Extraction of the linear model

STEP 2: COLD FET MEASUREMENTS (Optional):

Vgs: Channel Closed; Vds=0V

Channel pinch-off conditions

\[ C_{pd} = (\text{Im}(Y_{22}) + \text{Im}(Y_{21})) / W \]

\[ C_{pg} = (\text{Im}(Y_{11}) + 2*\text{Im}(Y_{21})) / W \]
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STEP 3: HOT FET (S parameters @ Quiescent bias point)

Set min. and max. for each extrinsic parameter
- user choice
- initiated by cold FET meas.

Optimization algorithm: annealing, fast simulated diffusion
(intrinsic parameters calculus)
STEP 3: HOT FET (S parameters @ Quiescent bias point)

- The selection of several plots enable to get rid off unrealistic solutions (Resistance >=0 only)
- Optimization can be launched simultaneously for all the points selected
- Each linear model has the same extrinsic values
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Compact model of GaN transistor (on-wafer)
Nonlinear model extraction

Small-Signal

Non-linear capacitances

IV Model

Thermal model

Trapping effects

Rg, Lg, Cpg, Ls, Cpd, Ld, Rs, Rd

Ri, Cds, τ, Gm, Gd, Cgs, Cgd, Rgd

Dgs=f(Vgs)
Dgd=f(Vgd)
Ids=f(Vgs,Vds)

Dgs=f(Vgs,T)
Dgd=f(Vgd,T)
Ids=f(Vgs,Vds,T)

Ids=f(Vgs_trap,Vds,T)

Rs=f(T)
Rd=f(T)

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Compact model of GaN transistor (on-wafer)

- 1 dimension capacitances extracted along optimal load-line are preferred due to simplicity.
- 1D capacitance models with equations based on hyperbolic tangents are naturally charge conservatives.
- Output Capacitance Cds is linear – no voltage dependence (weak anyway)

\[ C_{gd} = f(V_{gd}) \]  
\[ C_{gs} = f(V_{gs}) \]  
\[ \frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}} \]  
- Modeling simplicity. Very good convergence.
- The charges in the transistor are conservatives.
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Compact model of GaN transistor (on-wafer)

Cgd

- Feedback capacitance Cgd is a strong function of drain voltage.

\[ V_{gd} = V_{gs} - V_{ds} \approx -V_{ds} \]

GaN devices

Non linear capacitances

C0
C1
C2
A
B
Vm
Vp

Vgs variation

Intrinsic Vgd

Cgd

GaN devices

Measure
Model

Vgd = Vgs - Vds \approx -Vds
Cgs  Input capacitance Cgs is a strong function of gate voltage.

The gate-voltage non-linearity also effects model’s harmonic generation.
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IV model

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Trapping effects

Rg, Lg, Cpg, Ls, Cpd, Ld, Rs, Rd

Ri, Cds, \tau, Gm, Gd

Rg=f(T)

Rd=f(T)

Dgs=f(Vgs, T)

Dgd=f(Vgd, T)

Ids=f(Vgs, Vds, T)

Ids=f(Vgs_trap, Vds, T)

Cgs=f(Vgs)

Cgd=f(Vgd)

Cgs=f(Vgs)

Cgd=f(Vgd)

Rs=f(T)

Rd=f(T)
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Compact model of GaN transistor (on-wafer)

Selection of curve without Gate Current + 1 or 2 curves With Gate current

\[ I_{Gd} = I_{SGd} \cdot \left( e^{\left( \frac{G \cdot Vd}{N_{gd} \cdot K \cdot T} \right)} - 1 \right) \]

\[ I_{Gs} = I_{SGs} \cdot \left( e^{\left( \frac{G \cdot Vd}{N_{gs} \cdot K \cdot T} \right)} - 1 \right) \]

• Gate-drain and gate-source diode equations include forward conduction of gate current
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Compact model of GaN transistor (on-wafer)
IV model : output current

- AMCAD drain current model formulation allows to predict very accurately the I-V curves, the partial derivatives gm and gd, the knee voltage and the transconductance decrease at high current.

M, P ↔ fitting parameters
AlphaGm, Vgm, BetaGm, Vdm ↔ gm (derivative)
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Compact model of GaN transistor (on-wafer)

Electro thermal model

Small-Signal

Non-linear capacitances

IV Model

Thermal model

Trapping effects

\[ y = 0.0029x + 0.6375 \]
\[ y = 0.0049x + 0.6889 \]

\[ y = -0.0008x + 1.1543 \]

\[ R_s, R_d \]

\[ R_{g}, L_{g}, C_{pg}, L_s, C_{pd}, L_d, R_s, R_d \]

\[ R_{i}, C_{ds}, T, G_{m}, G_{d}, C_{gs}, C_{gd}, R_{gd} \]

\[ D_{gs} = f(V_{gs}) \]
\[ D_{gd} = f(V_{gd}) \]
\[ I_{ds} = f(V_{gs}, V_{ds}) \]

\[ D_{gs} = f(V_{gs}, T) \]
\[ D_{gd} = f(V_{gd}, T) \]
\[ I_{ds} = f(V_{gs}, V_{ds}, T) \]

\[ I_{ds} = f(V_{gs\_trap}, V_{ds}, T) \]

\[ R_{s} = f(T) \]
\[ R_{d} = f(T) \]
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Compact model of GaN transistor (on-wafer)

• Temperature dependence with ambient or chuck temperature
  -40°C
  25°C
  150°C

• Static and Dynamic self-heating effects

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Compact model of GaN transistor (on-wafer)
Electro thermal model

Temperature dependence

Equations

Thermal parameters
- Access Resistances
- Current Source
- Diodes

Rs = Rs₀ + α₁ Rs₁ T
Rd = Rd₀ + α₁ Rd₁ T
Idss = Idss₀ + Idss₁ T
P = P₀ + P₁ T
Ngs = Ngs₀ + Ngs₁ T
Ngd = Ngd₀ + Ngd₁ T
Isgs = Isgs₀ + Isgs₁ e(T/Tgs)
Isgd = Isgd₀ + Isgd₁ e(T/Tgd)
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Compact model of GaN transistor (on-wafer)

Thermal resistance extraction → coincidence method

\[ I_{ds} \quad \text{same } V_{gs} \]

\[ \begin{align*}
DC, \ T_{chuck1} &= 25^\circ C \\
Pulsed \ from \ (0,0), \ T_{chuck2} &= 100^\circ C \\
\end{align*} \]

\[ \begin{align*}
\text{DC curve} \\
T_{j1} &= T_{chuck1} + R_{th} P_{diss1} \\
\text{Pulsed curve} \\
T_{j2} &= T_{chuck2} + R_{th} P_{diss2} \\
\end{align*} \]

At intersection point

\[ T_{j1} = T_{j2} \]

\[ T_{chuck1} + R_{th} P_{diss1} = T_{chuck2} \]

\[ \Rightarrow \]

\[ R_{th} = \frac{(T_{chuck2} - T_{chuck1})}{P_{diss1}} \]
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Compact model of GaN transistor (on-wafer)

Electro thermal model

Thermal impedance extraction – by measurements

Wide current pulse characterization

Wide pulse characterization (1.2ms) at 25°C from (0,0) -> Zth

Self Heating Extraction = f(t)

\[ i(t) = I_0 - \sum_{i=1}^{n} I_i \left( 1 - \exp \left( -\frac{t}{\tau_i} \right) \right) \]

\[ Z_{th}(t) = \sum_{k=1}^{n} R_{kth} \left( 1 - e^{-\frac{t}{R_{kth}C_{kth}}} \right) \]

RC cells

Device dynamical self-heating

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Compact model of GaN transistor (on-wafer)

- Drain current is only temperature dependent model element
- Takes into account ambient temperature and self-heating effects
- Thermal analog circuit to model self-heating and elevated heat sink temperatures
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Compact model of GaN transistor (on-wafer)

Trap model

- Charging and discharging of traps has influence on $I_D$ and leads to current collapse. This is described in the model by trapping effects modifying the gate command and separated into gate and drain lag sub-circuits.
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Compact model of GaN transistor (on-wafer)

Trap model

**Gate-lag: decrease of drain current**
- green ($V_{gs0} = 0\, \text{V}, V_{ds0} = 0\, \text{V}$)
- red ($V_{gs0} = -4\, \text{V}, V_{ds0} = 0\, \text{V}$)

**Drain-lag: increase of V_knee**
- red ($V_{gs0} = -3\, \text{V}, V_{ds0} = 0\, \text{V}$)
- green ($V_{gs0} = -3\, \text{V}, V_{ds0} = 30\, \text{V}$)

$T_{\text{capture}} << t_{\text{IMPUSION}} << T_{\text{émission}}$

**During the pulses capture takes place, emission freezed**
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Compact model of GaN transistor (on-wafer)

Trap model

Measurements to extract Drain-lag at very low dissipated power
Compact model of GaN transistor (on-wafer)

**Trap model**
- Decreasing form of the mean output current only reproduced with traps accurately modeled.

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**Graphs and Data**
- **Ids (A)** vs. **Pin (dBm)**
  - Measured data (×)
  - Model without traps (red)
  - Model with traps (blue)

- **Pout (W)** vs. **Pin (W)**
  - Measured data (×)
  - Model without traps (red)
  - Model with traps (blue)

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AMCAD Model / Microwave Office
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DC simulation
Transistor Compact modeling using IVCAD

S parameter simulation
Transistor Compact modeling using IVCAD

HB simulation

[Diagrams of transistor compact modeling using IVCAD]
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AMCAD model -> ADS **

**Keysight Technologies
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AMCAD Model / ADS
Transistor Compact modeling using IVCAD

DC simulation
Transistor Compact modeling using IVCAD

S parameter simulation
Transistor Compact modeling using IVCAD

Thank you

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References


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