

Compact Transistor Models: The Roadmap to First-Pass Amplifier Design Success

Amplifier designers have been making use of modern transistor models since their first appearance in the mid-1970s. Models have allowed engineers to create advanced designs with first-pass success, without the need for multiple prototypes and design iterations. But with so many different modeling techniques, how does one select which one to use? The three most common types of models used in industry today are: physical models, compact models and behavioral models.

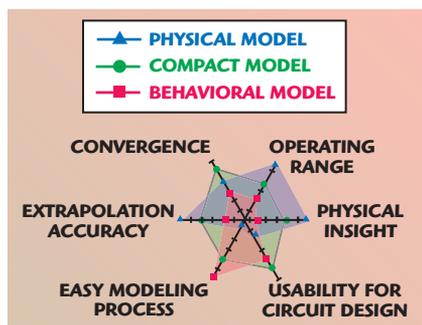
Physical models, as their name suggests, are based on the physics of the device technology. These models are dedicated to the transistor itself and not the overall circuit. Due to the nature of the model, complex model equations have to be used, which can lead to time-consuming simulations. The advantage of the

physical model is that it can be successfully used over the largest operating range, compared to alternate methods, since equations are used to describe complex physical rules rather than actual measurement results.

Compact transistor models, based on measured IV and S-parameters, allow designers to shift focus from transistor de-

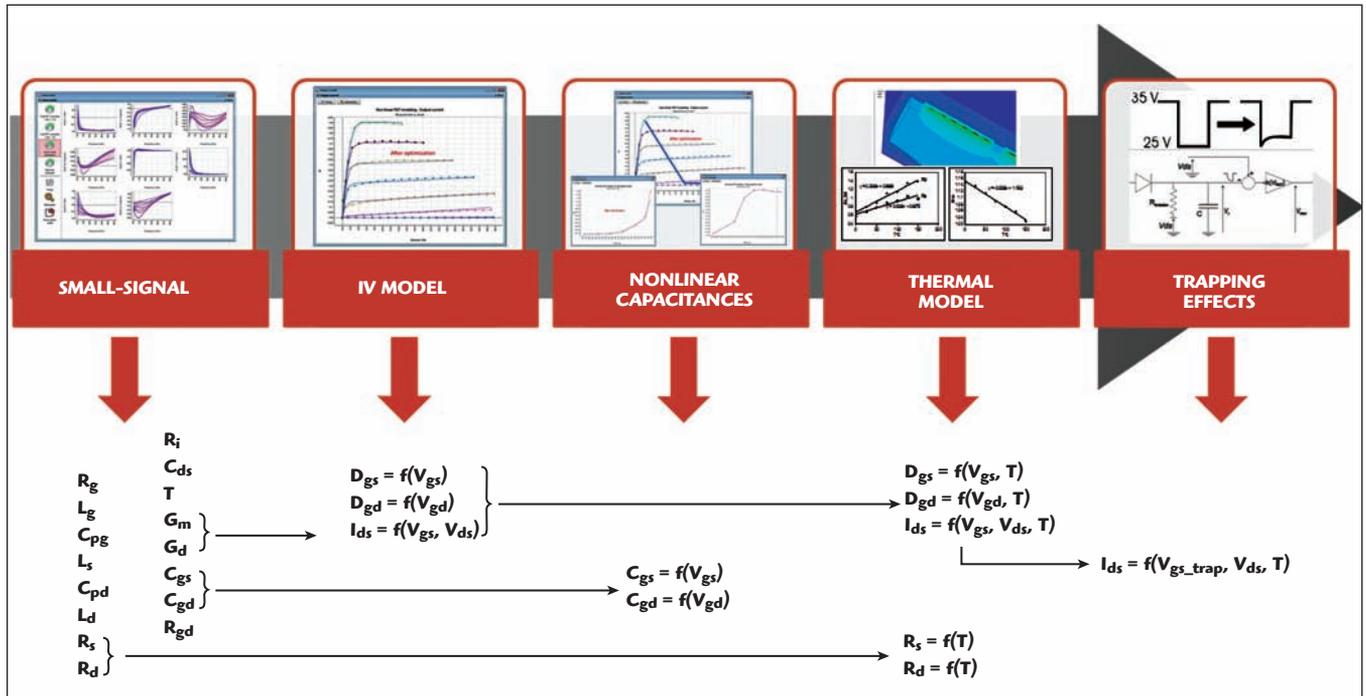
signs to circuit designs. Extracted from quasi-isothermal pulsed IV and pulsed S-parameter data and validated with load-pull characterization, compact transistor models contain a reduced set of parameters. Unlike other model types, compact models take into account complex phenomena, such as electro-thermal and trapping effects. For simulations under nonlinear operating conditions, responses to complex modulated signals (such as EVM or ACPR) are accurately predicted as low-frequency and high-frequency memory effects are taken into account. Compact transistor models are ideal for die-level applications, as developing such a model from IV and S-parameters is straightforward and relatively quick. Packaged-transistor models need to include a die-level model as well as a bonding model and package model, and consequently can be time consuming and costly.

Behavioral models, based on frequency domain measurements, are far less flexible than physical or compact transistor models, but can be easily developed for any type of component (including die-level or packaged transistors). Behavioral models are considered “black-box” models, where only the responses of the com-

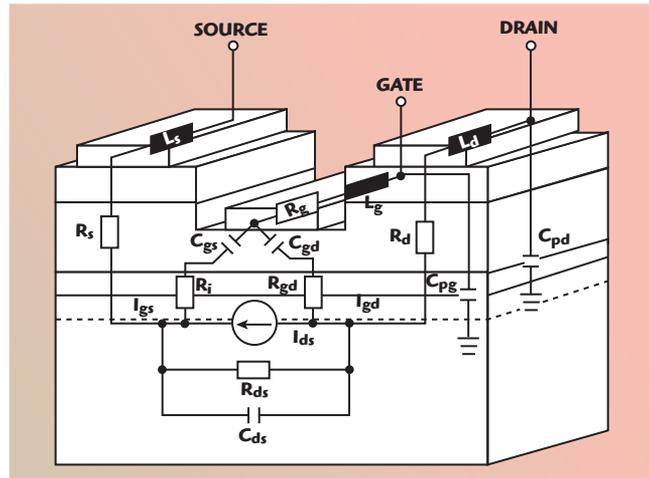


▲ Fig. 1 Type of large-signal models.

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▲ Fig. 2 Compact FET model extraction flow.



▲ Fig. 3 Compact FET model schematic.

ponent to some controlled stimuli are known, and are consequently only valid under the operating conditions measured. This model type is actively under development and has been recently improved to take into account memory effects,^{1,2} however, as a table-based model, it cannot be as complete as a formula-based model.

It is clear that each model type, physical, compact and behavioral, has unique advantages and disadvantages, as illustrated in **Figure 1**. While there is no one-size-fits-all model, compact transistor models offer the shortest development time for maximum flexibility with regards to die-level transistors.

Research and development of com-

compact transistor models has been, and continues to be, an important topic for universities and institutes across the globe.³⁻⁹ As such, an abundance of literature and documentation exists on the background R&D of compact models. This discussion will concentrate on the main topics involved with model extraction of wide band gap (WBG) field effect transistors (FET) such as gallium nitride (GaN) FETs. The perfect GaN compact transistor model needs to be accurate for device operation over temperature, bias and RF power. The design flow of a GaN FET compact transistor model, shown in **Figure 2**, consists of:

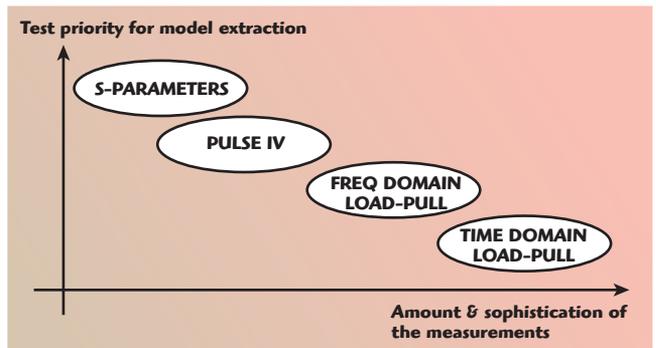
- Linear model extraction through small-signal S-parameters
- Nonlinear model extraction

- through pulsed IV measurements
- Nonlinear capacitance modeling through synchronized pulsed IV/RF
- Electro-thermal modeling through temperature control
- Trapping effect modeling

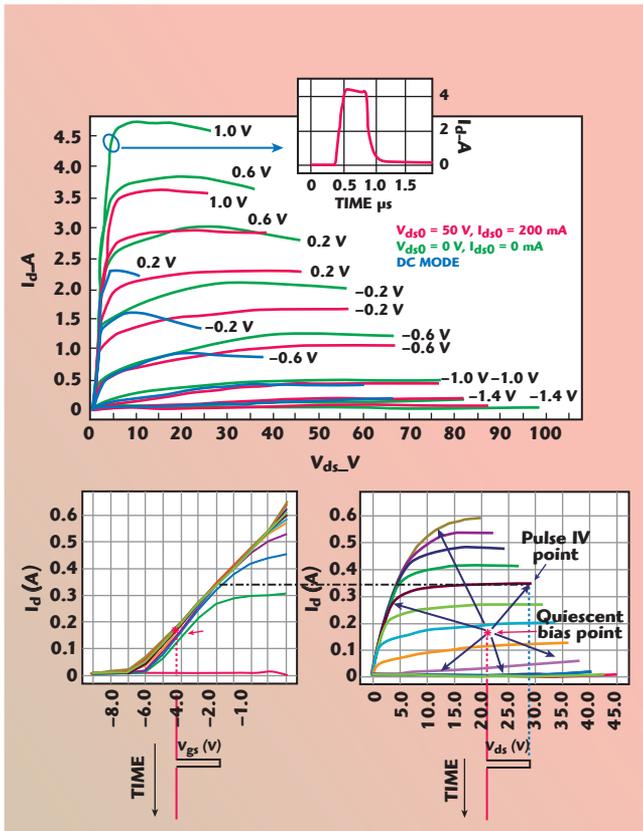
Additionally, the compact transistor model can be validated through load-pull measurements.

LINEAR MODEL EXTRACTION

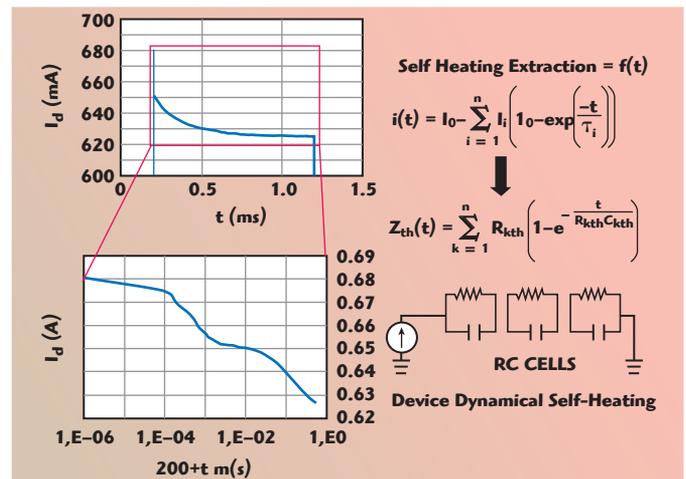
The first step in linear model extraction is to use S-parameters to determine the transistor's extrinsic parasitic elements (R_g , L_g , C_{pg} , R_d , L_d , C_{pd} , R_s and L_s), as sketched in **Figures 3** and **4**. By defining a set of extrinsic elements, the S-parameter data can be de-embedded to the intrinsic reference plane and a set of intrinsic parameters (C_{gs} , C_{gd} , G_m , G_d , C_{ds} , R_i , T_{au} , R_{gd}) can be extract-



▲ Fig. 4 Measurements for compact model.



▲ Fig. 5 DC and pulsed IV characteristics.



▲ Fig. 6 Thermal model extraction.

ed using explicit equations.¹⁰⁻¹¹

During the optimization process, the goal of the linear modeling step is to determine values for the extrinsic parameters, which in turn provides a set

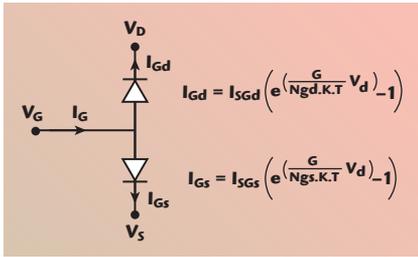
of intrinsic parameters with a fixed value versus frequency. During the modeling optimization, measured and modeled S-parameters are compared over the entire RF bandwidth. The measured S-parameters are converted to the corresponding [Y] and [Z] parameters, so that both [Y] and [Z] parameters can be compared at both intrinsic and extrinsic reference planes.

NONLINEAR MODEL EXTRACTION WITH PULSED IV

Nonlinear model extraction uses pulsed IV measurements to study the effects of temperature-dependent performance (including self-heating) in safe operating regions and to study the breakdown area of the transistor (see **Figure 5**).¹² Pulse widths are kept sufficiently short in order to avoid a strong temperature variation during the pulse duration and the duty cycle is kept sufficiently low in order to avoid a mean variation of the temperature, so that the transistor's pulsed IV measurements are obtained under quasi-isothermal operating conditions.

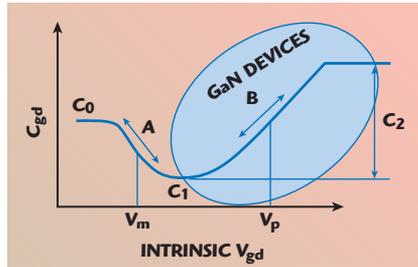
It is necessary to determine the transistor's thermal impedance in order to complete an electro-thermal model that can dynamically predict performance as a function of device temperature (chuck temperature) and self-heating.^{9,13} To extract the thermal impedance, two sets of measurements are performed.

First, IV measurements are performed under both continuous (DC) and short-pulsed conditions in order to extract the thermal resistance. As shown in **Figure 6**, longer pulses are



▲ Fig. 7 Gate current model.

then applied in order to study the current decrease with time and extract the thermal capacitance. How the temperature (and therefore performance) varies with time is related to the transistor's design, number of layers, type of carrier, heat sink, etc.; the thermal impedance can be modeled by a combination of several thermal resistances and several thermal capacitances representing various time constants. This thermal circuit provides the equivalent transistor junction temperature as a function of DC power and is used in the various sub-circuit models (resistances, current source, diodes and breakdown circuits) that are linked to voltages,



▲ Fig. 8 C_{gd} nonlinear capacitance.

currents and temperatures.

In the example shown in **Figure 7**, the input current diodes must be modeled by equivalent nonlinear current sources that are able to generate a positive gate current when the transistor is biased in forward model with low V_{ds} and high V_{gs} values, and able to generate a negative current for high V_{ds} and pinch-off V_{gs} values. To ensure convergence, the output current source model has to be continuous at n-order for any V_{gs} and V_{ds} values. The AMCAD-FET model uses a current source model that can be formulated using the following equations:

$$I_{ds} = U \tanh(\alpha V_{ds}) \quad (1)$$

$$\alpha = \frac{1}{2} \cdot$$

$$\left((\alpha_1 - \alpha_2) \tanh(-V_{gs} + V_{g1}) + (\alpha_1 + \alpha_2) \right) \quad (2)$$

$$U = Fa \cdot$$

$$\left(I_1 (V_1 + \lambda) + \frac{(V_{ds} - V_{dsp})}{R_{ds0}}, R_u, U_0 \right) \quad (3)$$

$$V_1 = F_p (V_{gs}, V_{ds}) \quad (4)$$

where α_1 , α_2 , V_{gs1} , I_1 , λ , V_{dsp} and R_{ds0} are parameters. The "Fa" function defines a lower limit to a related function from an arbitrary value U_0 with an adjustable smooth transition parameter R_u . The "F_p" function is an n-order polynomial with two variables (V_{gs} , V_{ds}). Additionally, measurements can be repeated at various chuck temperatures when measuring on-wafer. This allows a temperature-dependence variable to be determined and applied to the model.

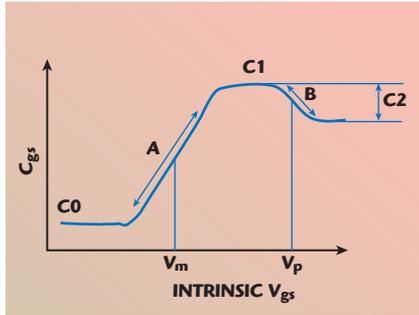
NONLINEAR MODEL EXTRACTION WITH PULSED IV/ PULSED RF

Nonlinear capacitance modeling, determining C_{gd} and C_{gs} models, is achieved through synchronized pulsed RF (Pulsed S-parameters) and pulsed bias (Pulsed IV) measurements along with the predicted RF load line. While nonlinear capacitances can be modeled by equations that depend on both V_{gd} and V_{gs} voltages concurrently (referred to as two-dimensional models), it has been shown that one-dimension capacitance models are more robust regarding convergence without sacrificing accuracy.¹⁴ The C_{gd} capacitance model is therefore linked with V_{gd} while the C_{gs} capacitance model relies on V_{gs} .

The feedback capacitance C_{gd} depends heavily on the drain voltage; therefore, it must be included to fit large-signal operating conditions. The C_{gd} capacitance model is defined by the equation

$$C_{gd} = C_{gd0} + \frac{C_{gd1} - C_{gd0}}{2} \cdot \left[1 + \tanh\left(c(V_{gd} + V_n)\right) \right] - \frac{C_{gd2}}{2} \left[1 + \tanh\left(d(V_{gd} + V_q)\right) \right] \quad (5)$$

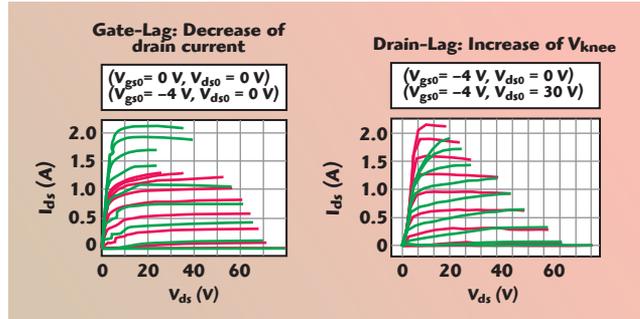
This one-dimension C_{gd} capacitance model, shown in **Figure 8**, was



▲ Fig. 9 C_{gs} nonlinear capacitance.

initially optimized for gallium arsenide (GaAs) transistors, but has been updated for GaN technologies. Along the same RF load line, the one-dimension input capacitance model C_{gs} , shown in **Figure 9**, depends heavily on gate voltage. The gate voltage's nonlinearity greatly affects the model's harmonic response. The capacitance can be modeled by the equation

$$C_{gs} = C_{gs0} + \frac{C_{gs1} - C_{gs0}}{2} \left[1 + \tanh\left(a(V_{gs} + V_m)\right) \right] - \frac{C_{gs2}}{2} \left[1 + \tanh\left(b(V_{gs} + V_p)\right) \right] \quad (6)$$



▲ Fig. 10 Trapping effects.

The output capacitance C_{ds} is linear; no voltage dependence is taken into account due to the weak influence for amplification purposes.

TRAPPING EFFECTS

Nonlinear model extraction also takes advantage of pulsed IV measurements to isolate the trapping effects as a function of quiescent bias condition. Trapping effects are parasitic effects that reduce the maximum output current; the charging and discharging of traps influences I_{ds} and leads to current collapse. Trapping corresponds to the existence of energy states, which can be occupied by holes or electrons

in the gap. These holes or electrons are trapped at these levels over a time period and cannot take part in conduction, hence the term trap. Trapping is the result of impurities or defects in the crystalline network of the material from which the transistor is composed, and alters

the electric behavior of the transistor at microwave frequencies.

Pulsed IV measurements are used to study the individual trapping effects and differentiate between surface trapping (gate-lag) and buffer trapping (drain-lag). When performing pulsed IV measurements, it is important to ensure the IV pulses are shorter than the emission time constant of the traps. It is also important to maintain a constant temperature throughout the measurement to be certain that the device changes are due to trapping effects and not temperature changes.

Gate-lag is mainly attributed to surface trapping effects. In order to isolate these effects, two series of measurements are made with identical dissipated powers equal to zero. When performing pulsed IV measurements, the two quiescent bias points chosen are:

$$\begin{aligned} \text{QP1} : V_{gs0} &= V_p, V_{ds0} = 0 \text{ V} \\ \text{QP2} : V_{gs0} &= 0 \text{ V}, V_{ds0} = 0 \text{ V} \end{aligned}$$

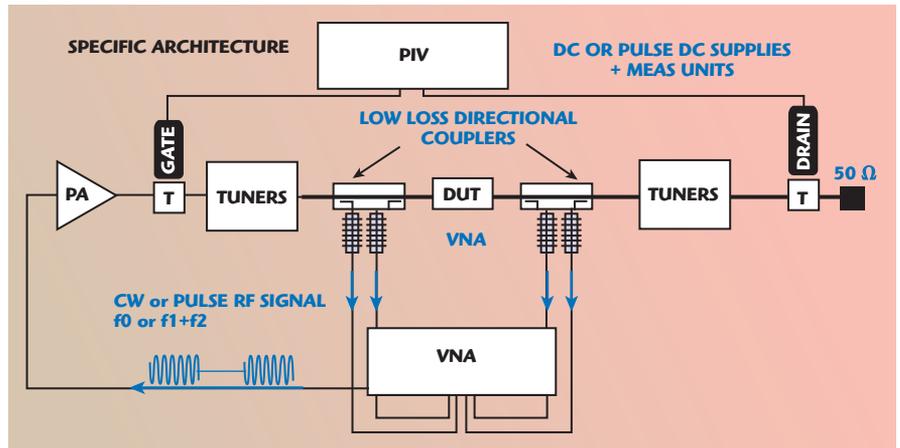
V_p is the pinch-off voltage applied on the gate. Because both dissipated powers are zero, any difference between IV characteristics can be attributed to the presence of gate lags.

Drain-lag is mainly attributed to buffer trapping effects. In order to isolate these effects, two series of measurements are made with identical dissipated powers equal to zero. When performing pulsed IV measurements, the two quiescent bias points chosen are:

$$\begin{aligned} \text{QP1} : V_{gs0} &= V_p, V_{ds0} = 0 \text{ V} \\ \text{QP3} : V_{gs0} &= 0 \text{ V}, V_{ds0} \gg 0 \text{ V} \end{aligned}$$

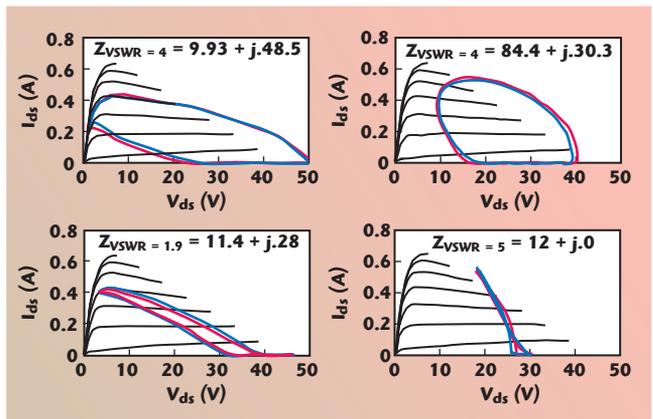
Examples of typical gate-lag and drain-lag IV curves are shown in **Figure 10**.

These parasitic phenomena can be modeled by a trapping circuit composed of gate- and drain-lag sub-



▲ Fig. 11 VNA-based load pull setup.

circuits that are connected to the gate command¹⁵ in order to drive the output current as a parasitic phenomenon. The lagging hysteresis can be modeled by a circuit that contains a diode element that will reproduce the dissymmetry between the capture and emission times.¹⁶



▲ Fig. 12 Model validation.

LOAD-PULL FOR MODEL VALIDATION

Load-pull measurements are used to validate compact transistor models beyond 50Ω by varying the impedances presented to the transistor and comparing measured and modeled parameters. In order to achieve a good correlation between measured and modeled results, it is important to use a vector-receiver (real-time) load-pull system, as shown in **Figure 11**. Vector-receiver load-pull systems make use of a vector receiver calibrated at the device-under-test (DUT) reference plane to measure the transistor's large signal input impedance.¹⁷ Knowledge of the transistor input impedance removes the mismatch effect between the source impedance and the device impedance, allowing for a true power gain comparison. Power gain is directly related to the intrinsic transistor's performance contained within the model, whereas transducer gain is only an indicator of how the transistor is matched. The mismatch

between the source impedance and the transistor's input impedance can hide unstable operating conditions where the transistor's input impedance has negative values for certain load impedances,¹⁸ as the input impedance varies with power delivered to the input of the transistor. This input impedance measurement is important for model validation; during simulations, a model's effectiveness is judged by its ability to accurately predict power gain expansion and/or compression, which plays a major role in linearity.

Time-domain load-pull measurements may also be used for model validation.¹⁹ In addition to the parameters obtained from a frequency-domain system, time domain load-pull allows for the measurement of voltage and current waveforms and load lines. When correctly calibrated and de-embedded to the intrinsic transistor reference plane, the RF load line can be displayed and superimposed onto the transistor's IV characteristics, and a comparison between measured

and modeled results can be made, as shown in **Figure 12**. Time-domain voltage and current waveforms and load lines can be used to verify whether the transistor is operating close to RF breakdown, or used to confirm class of operation (A, AB, C, E, F, F-1, G...).

CONCLUSION

Amplifier designers are under more stress than ever to release effective products in the least amount of time and maximize profitability; meaning first-pass design success and being first-to-market. Gone are the days when engineers could cut and paste, design by trial and error, and work at their own pace to release innovative products. Compact transistor models are the first and most crucial step in a successful MMIC design flow and, when used in conjunction with circuit simulators, can lead to first-pass design success and first-to-market. ■

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